MON3100

Compact, Low-Power Wireless Baseband Processor

Overview

The MON3100 is a compact, low-power and reconfigurable processing platform aimed at wireless baseband signal processing applications. It is part of MAC Ltd's MONITOR product range and, when combined with an RF front-end, forms a complete software-defined receiver. By incorporating a variety of peripheral devices and interfaces it reduces system complexity by combining the functions of several modules onto a single board, thus reducing size and cost.

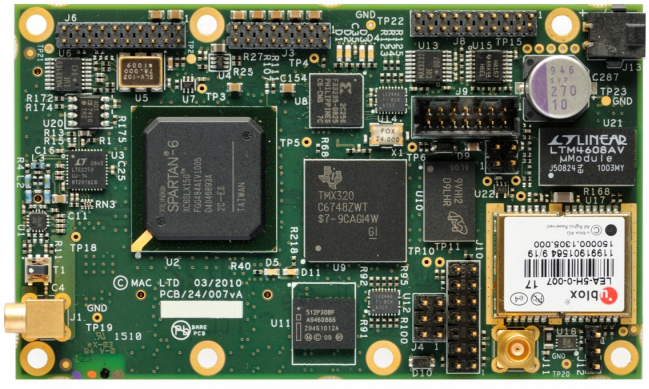
Features

- 140 MHz intermediate frequency input
- Up to 80 MSample/s sampling rate
- 150 k logic cell Xilinx Spartan 6 FPGA
- TMS320C6748 for signal processing and control
- High-speed 480 Mbit/s USB2 interface
- High-performance GPS module
- GPS-conditioned ADC clock
- Extensive LVDS and CMOS connectivity
- PC-controlled/standalone operation
- Applications development kit (ADK)

Applications

- RF measurement equipment
- High-speed data capture
- Software-defined radio
- High-speed spectral analysis
- Digital down-converters

The MON3100



Description

To provide significant processing power with low power consumption in a small package the MON3100 signal processing card is fitted with a XC6LX150 Spartan 6 FPGA and a TMS320C6748 DSP. Both of these devices offer a state-of-the-art trade-off between power consumption and performance.

This XC6LX150 FPGA includes 23040 'slices', 184 DSP48A1s (which include 18-bit × 18-bit hardware multipliers) and 268 18-Kbit random access memory (RAM) blocks. The FPGA also includes clock management primitives that can be configured to implement a number of useful functions including clock multiplication, division and phase realignment.

The FPGA is combined with a low power 32-bit Texas Instruments TMS320C6748 VLIW fixed/floating point DSP, which is clocked at up to 300 MHz and can achieve a peak performance of 2400 MMACs/s. Incorporated into this device are a number of useful peripherals including UARTs, SPI and I2C interfaces and a high-speed USB2 interface that is used as the primary control interface to the MON3100 signal processing card. Fast connectivity is provided to the FPGA via the universal parallel port (UPP) and the external memory interface (EMIFA). The UPP offers two independent 16-bit data paths, each supporting an aggregate transfer rate of up to 150 MByte/s.

Besides performing digital signal processing functions the DSP is also used as a control entity, performing tasks such as configuring the FPGA and controlling the various peripherals on the MON3100. The DSP can be configured to boot from a UART interface or from a 32-MByte non-volatile flash memory that, as well as DSP program data, can be used to store FPGA configuration data and application-specific user data. Thus, the MON3100 can configure itself without intervention from a host PC. The DSP's 256-KByte internal memory is augmented by an external 128-MByte DDR2 synchronous dynamic RAM (SDRAM).

The MON3100 signal processing card can accept an analogue IF input, which is sampled using a low-power, high-performance, 14-bit ADC (LT2258-14). An onboard, GPS-conditioned VCXO provides a low phase-noise, fixed-frequency sample clock for the ADC; the required sample clock frequency (typically in the range 60-64 MHz or 78-80 MHz) should be specified at the time of manufacture.

Other peripherals connected to the DSP include a high-performance u-blox LEA-6H GPS receiver, a 3-axis accelerometer, a temperature sensor, and a multichannel ADC for monitoring the onboard power supplies.

In addition to the dedicated interfaces, the MON3100 signal processing card provides a large number of general-purpose inputs and outputs (GPIO). These include buffered RS232-compatible signals, buffered 5 V-tolerant inputs and outputs as well as a number of non-buffered 3.3 V and 1.8 V GPIO. Many LVDS pairs are available on expansion headers, as are dedicated SPI and I2C interfaces to the DSP.

The MON3100 signal processing card measures 100 mm x 60 mm, and consumes less than 700 mA from a single 5.0 V supply when actively processing data in a typical application.

An applications development kit (ADK) that provides example FPGA, DSP and PC software to accelerate the process of creating user designs is available.

MONITOR Product Range

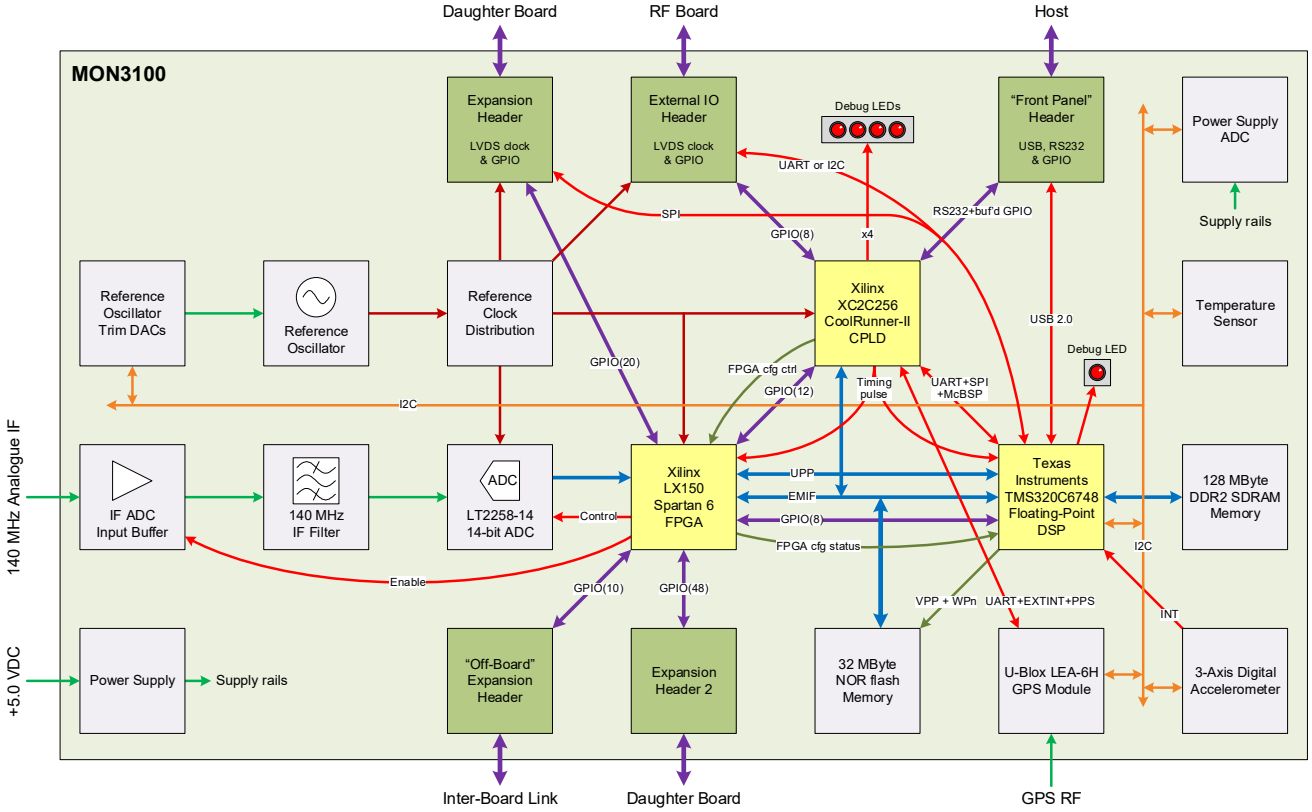
The MON3100 product family includes a companion single channel, tri-band receiver card, which provides a single conversion from RF to IF with up to 50 dB gain and a noise figure of 8 dB. A multi-channel transceiver card incorporating two pairs of phase-coherent receivers and a single channel direct-conversion transmitter is under development.

Further members of the family are planned and bespoke versions can be developed. Please ask for further details.

Ordering Information

To order please contact MAC Ltd at the address below. Custom versions of the MON3100 cards as well as a full software and FPGA design service are available on request. Please contact MAC Ltd for further details.

MON3100 Compact Low Power Wireless Baseband Processor Block Diagram



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